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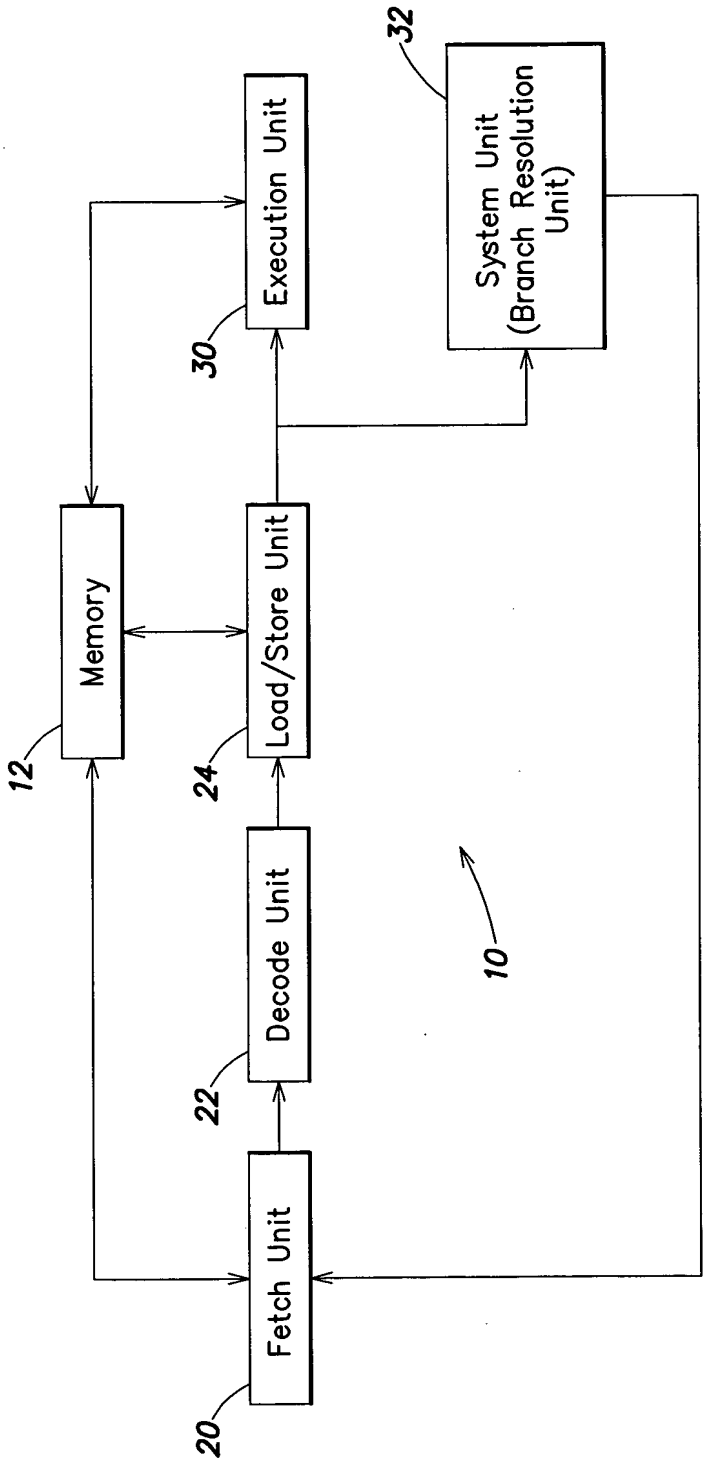

FIG. 1

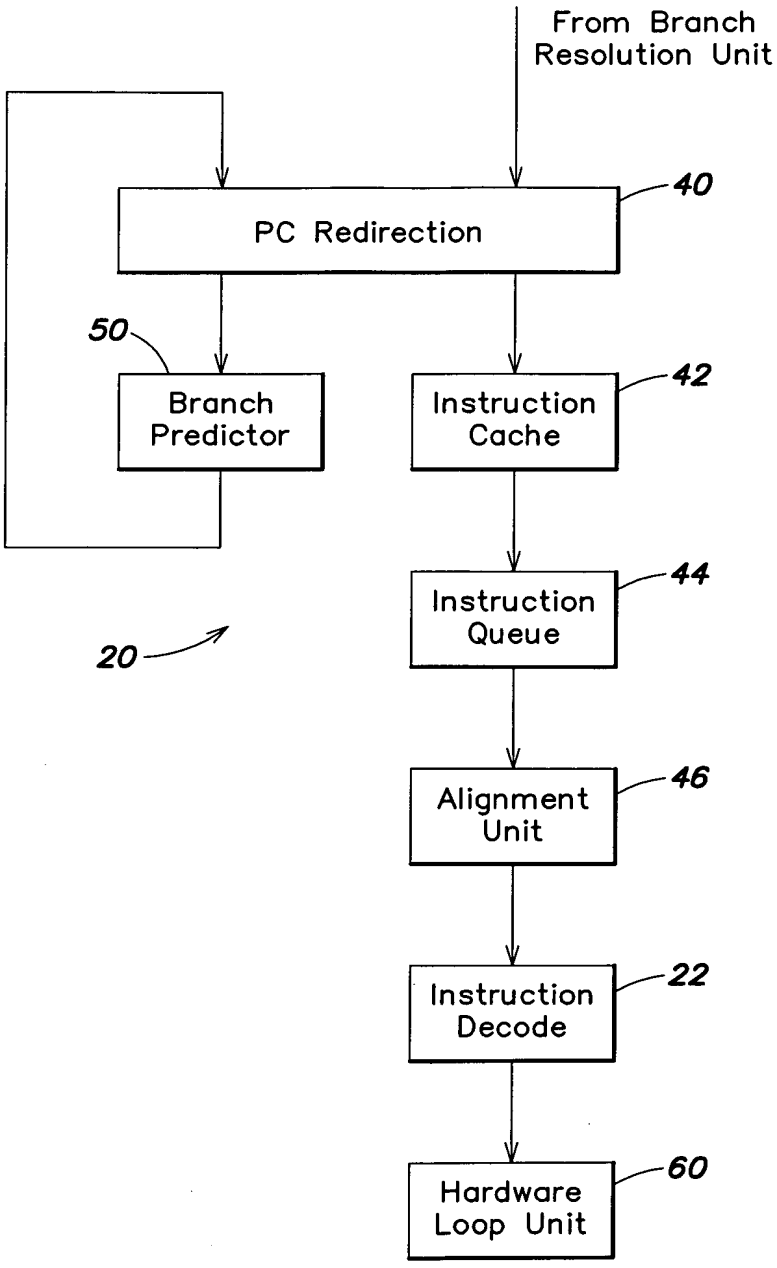
From Branch
Resolution Unit
PC Redirection
40
50
Branch
Predictor
Instruction
Cache
42
Instruction
Queue
44
20
Alignment
Unit
46
Instruction
Decode
22
Hardware
Loop Unit
60

FIG. 2

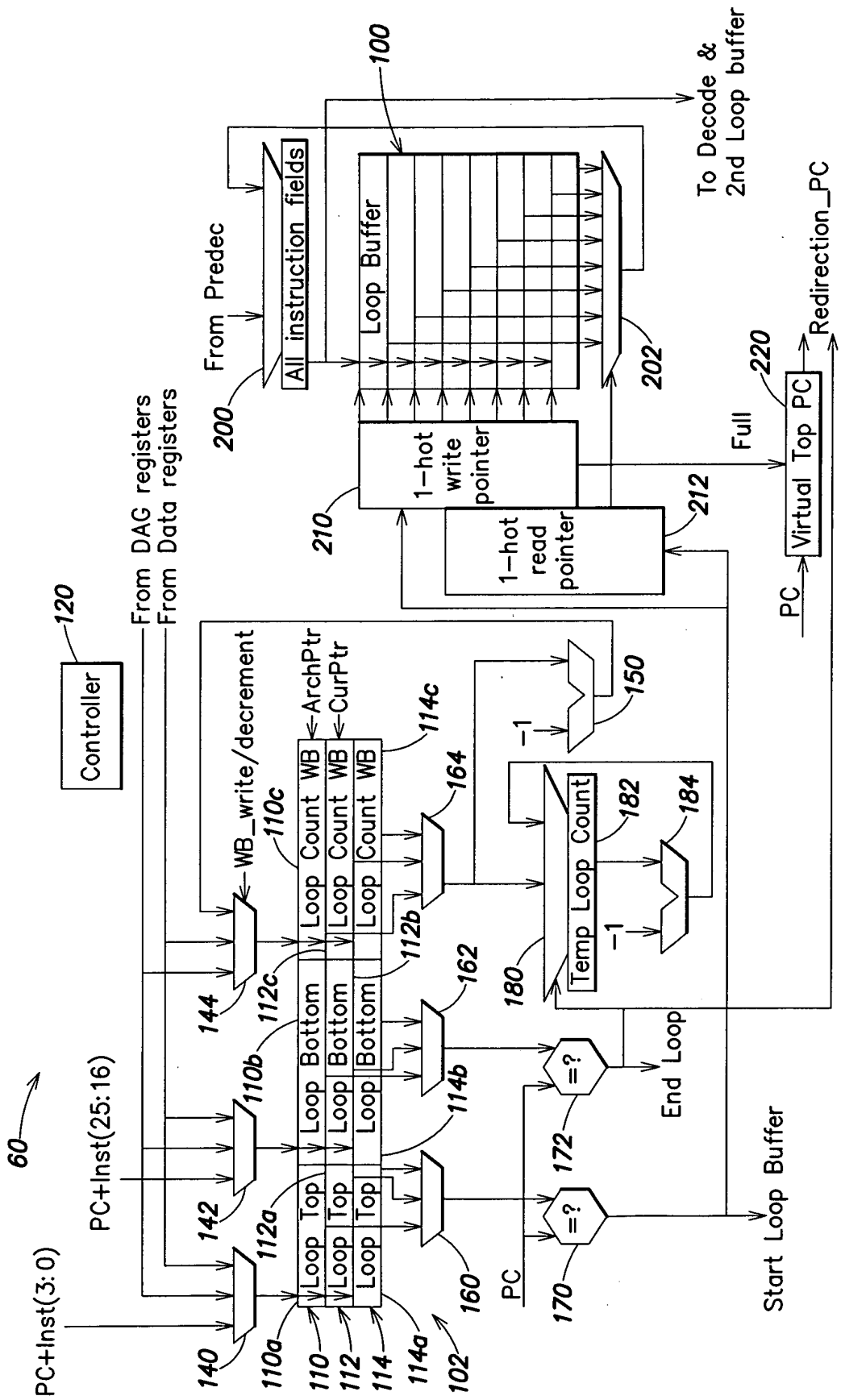
60
Controller
120
From DAG registers
From Data registers
From Predec
All instruction fields
200
Loop Buffer
100
202
To Decode &
2nd Loop buffer
1-hot write pointer
210
1-hot read pointer
212
Full
220
Virtual Top PC
Redirection_PC
PC
PC+Inst(25:16)
PC+Inst(3:0)
WB_write/decrement
ArchPtr
CurPtr
Loop Top
Loop Bottom
Loop Count WB
110
112
114
110a
112a
114a
110b
112b
114b
110c
112c
114c
102
140
142
144
160
162
164
150
-1
180
Temp Loop Count
182
184
=?
172
170
PC
End Loop
Start Loop Buffer

FIG. 3

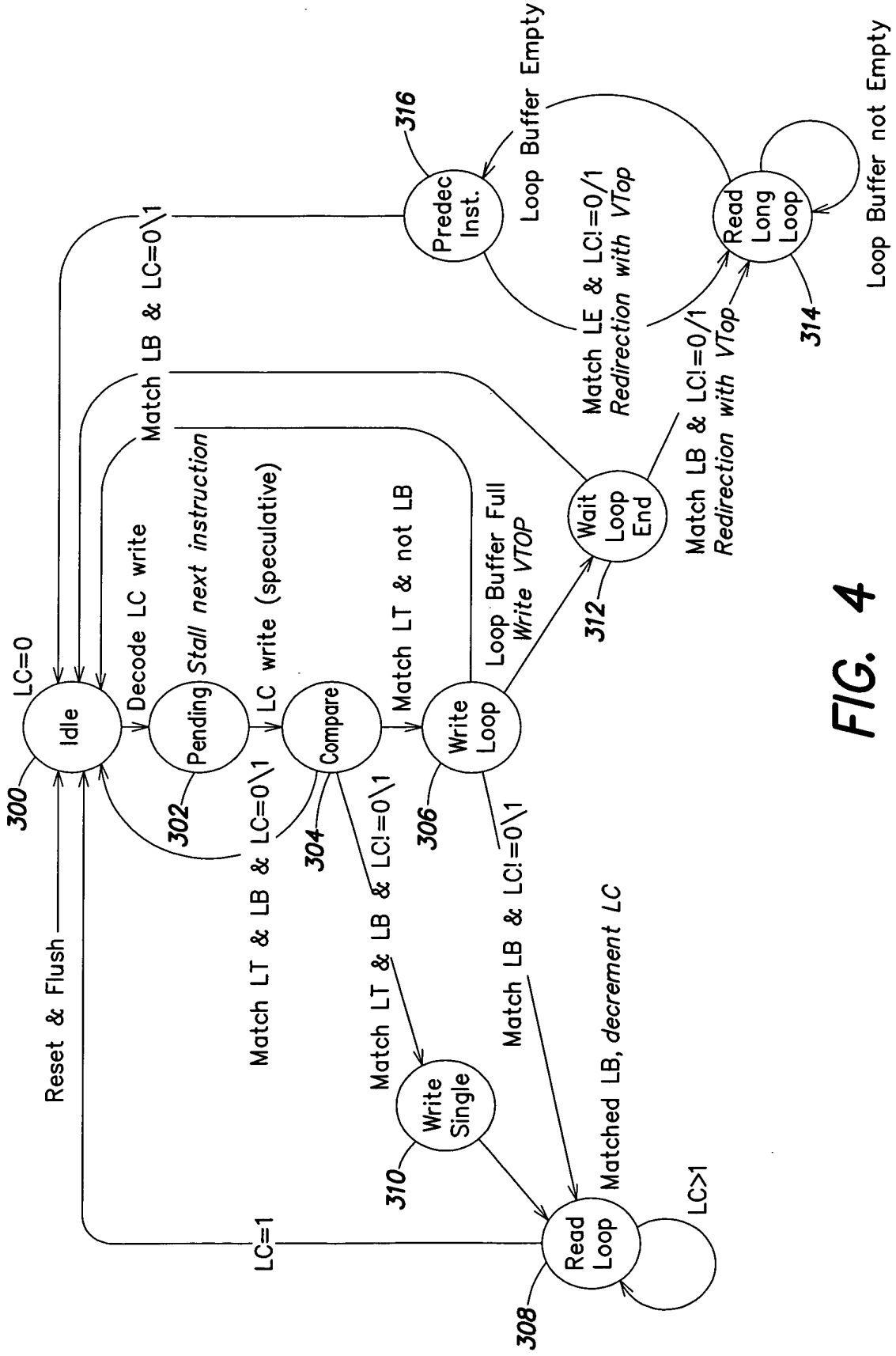
Idle
Pending
Compare
Write Loop
Wait Loop End
Predec Inst.
Read Long Loop
Write Single
Read Loop
300
302
304
306
308
310
312
314
316
LC=0
Reset & Flush
Decode LC write
Stall next instruction
LC write (speculative)
Match LT & not LB
Loop Buffer Full
Write VTOP
Match LB & LC=0\1
Match LT & LB & LC=0\1
Match LT & LB & LC!=0\1
Match LB & LC!=0\1
Match LB, decrement LC
Matched LB, LC=1
LC>1
Loop Buffer Empty
Loop Buffer not Empty
Match LE & LC!=0/1
Redirection with VTop
Match LB & LC!=0/1
Redirection with VTop

FIG. 4

	Inst	PC(7:0)	Inst Length	Offsets	Next PC	Loop Top	Loop Bottom	Loop Count	Loop Buffer	Comment
400	Lsetup	00110100	32-bit	2/16	00111000	00111000	01010100	Pending	Loopsetup	Loopsetup
401	I1	00111000	16-bit	–	00111010	Match	–	20	write I1	
402	I2	00111010	16-bit	–	00111100	–	–	20	write I2	
403	I3	00111100	16-bit	–	00111110	–	–	20	write I3	
404	I4	00111110	16-bit	–	01000000	–	–	20	write I4	
405	I5	01000000	16-bit	–	01000010	–	–	20	write I5	
406	I6	01000010	32-bit	–	01000100	–	–	20	write I6	
407	I7	01001000	32-bit	–	01001100	–	–	20	write I7	
408	I8	01001100	64-bit	–	01010100	–	–	20	write I8	
409	I9	01010100	16-bit	–	01010110	–	Match	20	write I9 read I1	set Vtop
410	I1	00111000	16-bit	–	00111010	Match	–	19	read I2	Fetch I9
411	I2	00111010	16-bit	–	00111100	–	–	19	read I3	

FIG. 5

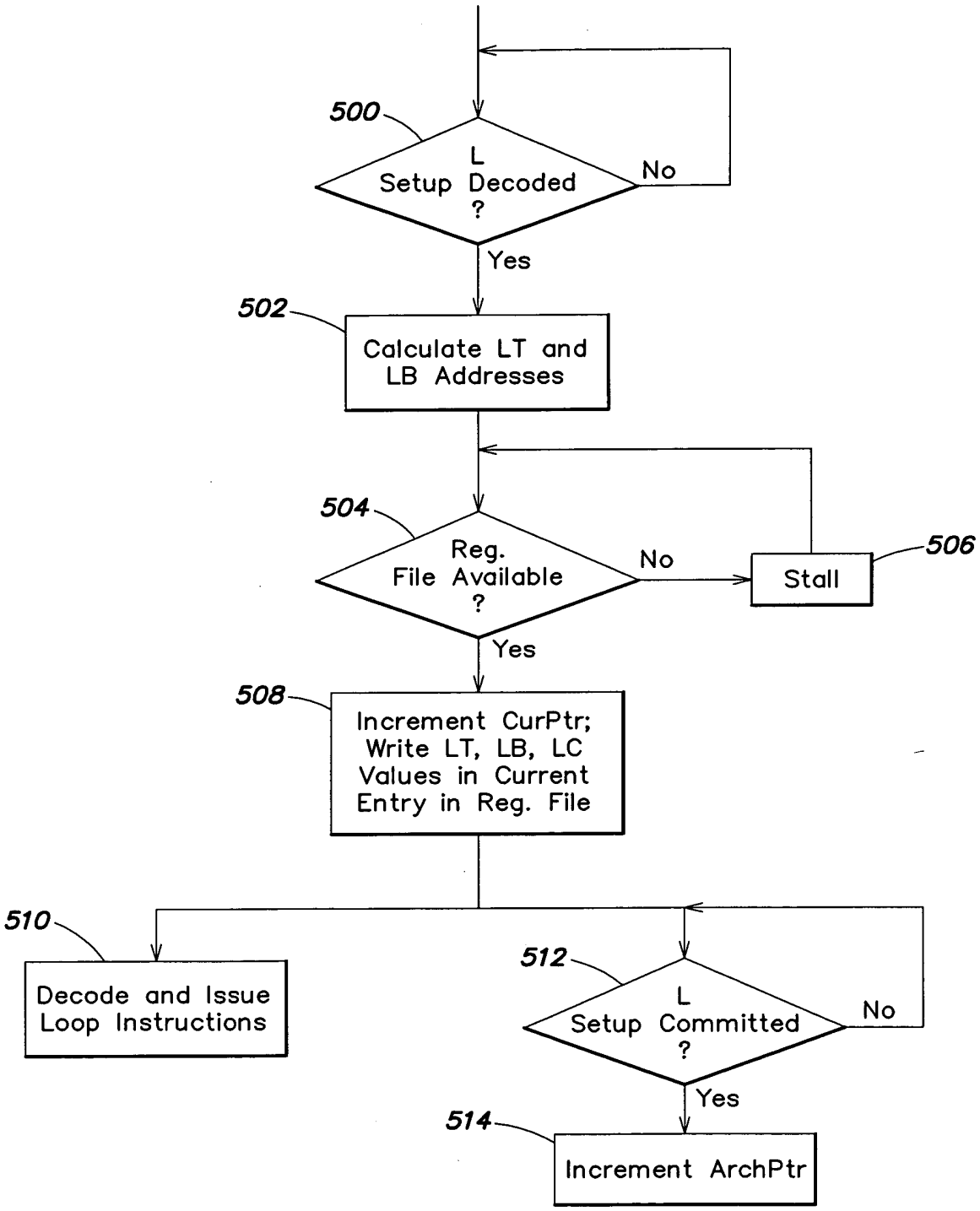
500
L Setup Decoded ?
No
Yes
502
Calculate LT and LB Addresses
504
Reg. File Available ?
No
506
Stall
Yes
508
Increment CurPtr; Write LT, LB, LC Values in Current Entry in Reg. File
510
Decode and Issue Loop Instructions
512
L Setup Committed ?
No
Yes
514
Increment ArchPtr

FIG. 6

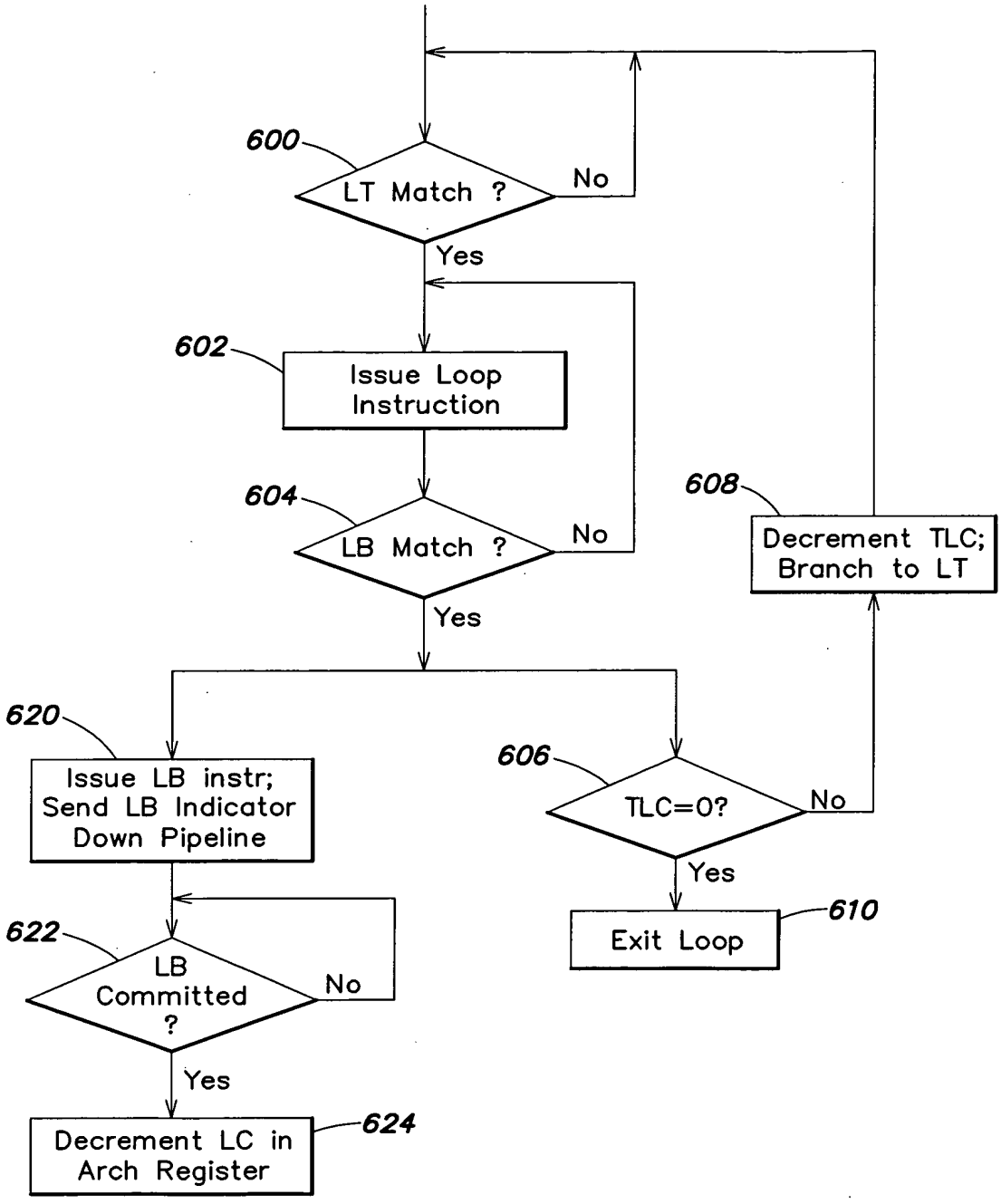
600
LT Match ?
No
Yes
602
Issue Loop Instruction
604
LB Match ?
No
Yes
608
Decrement TLC; Branch to LT
620
Issue LB instr; Send LB Indicator Down Pipeline
606
TLC=0?
No
Yes
610
Exit Loop
622
LB Committed ?
No
Yes
624
Decrement LC in Arch Register

FIG. 7

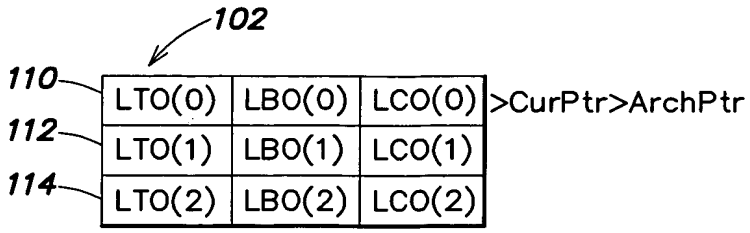

FIG. 8A

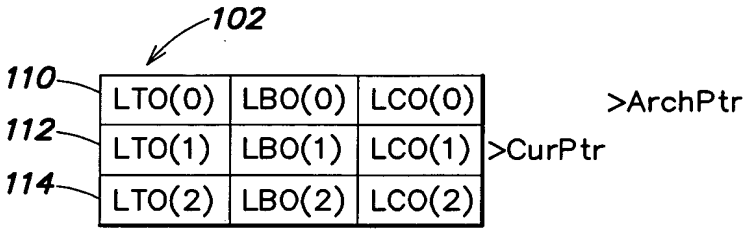

FIG. 8B

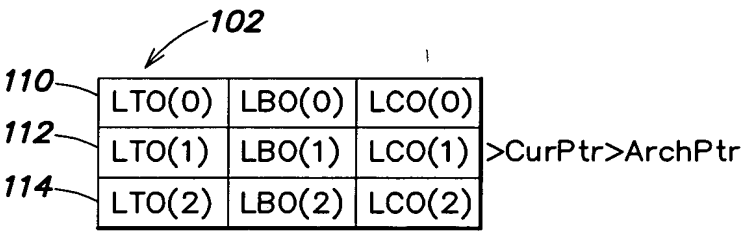

FIG. 8C

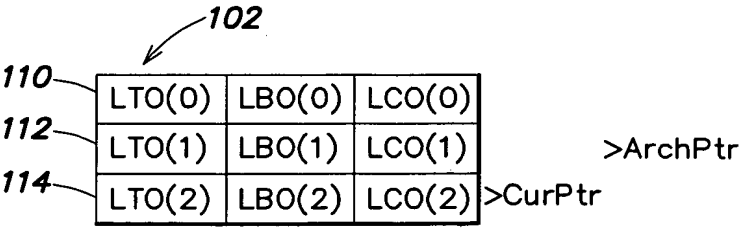

FIG. 8D

Pipe/Cycle	DEC	AC1	AC2	AC3	LS1	LS2	LS3	UC1	LT(0)/LB(0)	TLC/LC(0)	LT(1)/LB(1)	TLC/LC(1)
701 1	I1	Loop0							PC+2, PC+6	2,2		
702 2	I2	I1	Loop0						PC+2, PC+6	1,2		
703 3	I1	I2	I1	Loop0					PC+2, PC+6	1,2		
704 4	I2	I1	I2	I1	Loop0				PC+2, PC+6	0,2		
705 5	Loop1	I2	I1	I2	I1	Loop0			PC+2, PC+6	0,2		
706 6	I4	Loop1	I2	I1	I2	I1	Loop0		PC+2, PC+6	0,2	PC+2, PC+2	0,0
707 7	I5	I4	Loop1	I2	I1	I2	I1	Loop0	PC+2, PC+6	0,2	PC+2, PC+2	0,0
708 8	Loop2	I5	I4	Loop1	I2	I1	I2	I1	PC+2, PC+6	0,2	PC+2, PC+2	0,0
709 Interrupt	16	Loop	I5	I4	Loop1	I2	I1	I2	PC+2, PC+6	0,2	PC+2, PC+2	0,0
710 10		–	–	–	–	–	–	–	PC+2, PC+6	2,2	–	–

FIG. 9